DESCRIPTIVE CONTENT OF THE SUBJECT	

GENERAL INFORMATION		
Name:	**Complex digital systems design**	
ECTS credits:	**6**	
Semester:	**1st**	
Type:		**Compulsory**
Module:		**Telecommunication technologies**
Department:		**Electronic engineering and Automatic**
Area of knowledge:		**Electronic Technology**
Language:		**English**

Pre-requisites (if necessary)
There are no pre-requisites for this subject

ACTIVITIES AND ITS DISTRIBUTION IN ECTS CREDITS, METHODOLOGIES, AND LIST OF LEARNT COMPETENCES				
Activities/Methodologies	**ECTS Cr.**	**Attend. (hours)**	**Private work (hours)**	**Competences** (codes)
Lectures and tutorials:	3	30	45	TET2, TET3-TSC5
Lab work:	3	30	45	TET2, TSC3-TSC5
TOTAL	6,0	60	90	

LEARNING RESULTS	
Results 1	Having an overview of PLDs.
Results 2	Know how to use PLDs data sheets from manufacturers.
Results 3	Know the process and design tools with PLDs and FPGAs.
Results 4	Modelling digital circuits with ABEL and VHDL.
Results 5	Understanding the resources limitations of PLDs and FPGAs and know to select a device.
Results 6	Use CAD tools manufacturers to design complex digital circuits and systems with PLDs and FPGAs.

ASSESMENT METHOD			
Aspect	**Criteria**	**Instrument**	**Importance**
Attendance and participation	-Active participation in lectures and tutorials. - Active participation in lab work. -Attendance to individual tutorial and activities.	Observation.	10%
Subject concepts	-Practical and theoretical assimilation of subject concepts.	Written exam.	50%
Proposed works	-Documentation delivery. The revision for each document includes: - Structure - Quality - Novelty - Clarity of presentation	Revision of the documentation.	40%
The assessment method must fulfil the RD 1125/2003 of September the 5th in which is established the European system of credits and the assessment system for the academic studies with official character. The mark obtained in the topic “Subject concepts” has to be greater than 4 out of 10 in order to pass.			

SUBJECT SUMMARY
1. Programmable logic devices (PLDs) PLDs classification PLDs architecture CPLDs “ FPGAs “ 2. Digital design based on hardware description languages (HDL) HDL-based methodologies Design process Design tools 3. Hardware description languages: ABEL Source file structure Statements, operators, equations, extensions point. Tables, sequential circuits, state machines, test vectors, examples 4. Hardware description languages: VHDL Data types, operators Source file structure Ports, entities, architectures Description methods Combinational and sequential circuits State machines. Test environments VHDL design methodology 5. Design with CPLDs Synthesis Pin assignment Synthesis examples

Time model 6. Design with FPGAs XC4000 family architecture FPGA-oriented design Design process with Xilinx tools Design constraints 7. Lab work: ABEL design and assembly with SPLD VHDL design and assembly with FPGA